

#3 IDS 9/19/11
SHEET 1 OF 1

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 213672US2		SERIAL NO. NEW APPLICATION	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Kenji YAMAGUCHI, et al.			
				FILING DATE HEREWITH		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE, IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO	9-92700	4/4/97	Japan			X
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Narain D. ARORA, et al. "AN ACCURATE METHOD OF DETERMINING MOSFET GATE OVERLAP CAPACITANCE" Solid State Electronics Vol. 35, No. 12, 1992, pgs. 1817-1822					
	AX						
	AY						
	AZ						
Examiner <i>Harold B. Liguori-Puig</i>					Date Considered <i>6/17/2004</i>		

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*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.